REMARKS

Claims 1-4 are pending in this application. All claims are rejected under 35 U.S.C. § 103(a) as unpatentable over Rangan et al., U.S. Patent No. 6,147,634.

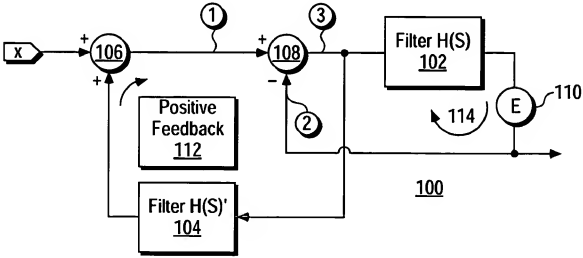
Claims 5-11 are newly added. They are supported by FIG. 1 and the examples of gain values at pp. 6-7 of the application.

Technology Tutorial

Applicants believe that a brief discussion of the technology disclosed in this application and the cited references would assist the Examiner, as the proposed modification of Rangan et al. would saturate, generate meaningless noise and not replicate the claimed invention.

This Disclosure

This disclosure combines positive feedback at input and negative feedback within a sigma delta modulator to reduce distortion in the ultimate signal output, as illustrated in FIG. 1.



The specification explains that the error source 110 is typically a quantizer. Applic. at 4:3-4.

The words of the claims refer to the positive feedback generated by adding an error voltage value using a **summation component configured to add** (106) and to negative feedback generated by subtracting a second error value using **a subtraction**

component configured to subtract (108). As between input at the left and output at the right, the addition (106) includes the input and the first error signal; the subtraction (108) includes the (input and first error signal) minus the second error signal.

The application includes an analysis in the s domain for a filter H(s)' that reduces the noise transfer function (NTF) by one-hundred fold. Applic. at 5-6.

Rangan et al. Reference

The Rangan et al. reference illustrates a conventional two stage sigma delta loop with negative feedback, without positive feedback.

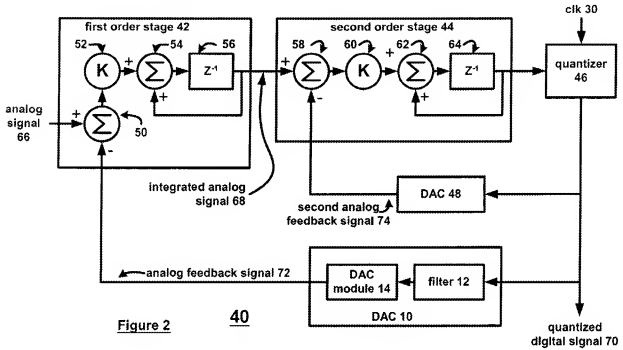
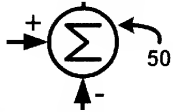


Figure 2 40

Negative feedback is applied at both stages, subtracting the first analog feedback signal (72) using the subtraction component (50) and subtracting the second analog feedback signal (74), using another subtraction component (58). Both of the error correction signals, taken from output of the quantizer (46) are applied as negative feedback.

The Examiner proposes (OA at 3:2-9) modification of the Rangan et al. circuit by changing the subtraction component (50) to an addition component. It is misleading at best to say, "The feedback signal of Rangan et al is distinctly shown ... applied to a summation circuit (50)", because the lower input marked "-" (minus sign.) ref. 50 plainly indicates subtraction instead of addition. Rangan's circuit would blow up if



modified to change subtraction to addition – that is, substituting positive feedback for negative feedback would immediately saturate the circuit and produce meaningless output at ref. 70.

There is no suggestion that modifying Rangan's circuit by substituting (ref 50) addition for subtraction would produce a 100-fold attenuation of the noise transfer function.

If the Examiner's proposed modification involves something other than simply modifying ref. 50 from subtract to add, Applicants would appreciate a sketch from the Examiner of the proposed modification. Words alone may not convey the Examiner's intended modification. Moreover, a few ambiguous words may conceal the extensive modifications that would be required to read on the claim.

Rejection Under 35 U.S.C. § 103(a) of Claims 1-4

The Examiner rejects **claims 1-4** under 35 U.S.C. § 103(a) as unpatentable over Rangan et al., U.S. Patent No. 6,147,634.

Claim 1

Claim 1 includes the limitations:

receiving an input signal;

adding a first error voltage value, which is derived from an output 5 signal, to the input signal;

subtracting a second error value, which is derived from the adding of a first error voltage value, to the input signal from the input signal; and

outputting an output signal result from the sigma delta circuit.

These limitations are not found in Rangan et al.

The Examiner bases this rejection on § 103(a) instead of § 102 (OA at 2-3) because Rangan et al. ref. 50 implements negative feedback; it is a subtraction component configured to subtract, not to add.

The Examiner's proposed modification is either to change the input to ref. 50 from "-" to "+" (minus to plus; subtract to add) or the Examiner's proposed modification

is so fatally indefinite that Applicants cannot be required to respond, that it does not make out a *prima facie* case.

The Examiner's proposed modification fails, as a matter of objective indicia of non-obviousness (the *Graham* factors), to render the technology disclosed obvious. The technology disclosed has been analyzed in the application as capable of reducing the NTF by 100-fold. The proposed modification of Rangan et al. would immediately saturate and produce meaningless output at ref. 70. One of skill in the art, motivated to suppress noise, would never implement or even attempt the modification that the Examiner proposes, because they would recognize how badly the modified circuit would operate.

Moreover, as modified, both of Rangan's first and second error signal come directly from the quantizer (46) and include the same errors. In contrast, claim 1 distinguishes the factors contributing the claimed first error signal and claimed second error signal. It is helpful to refer to FIG. 1 of this application, reproduced above, which illustrates taking first and second error signals from different points in the circuit.

As a matter of general principle, we remind the Examiner that real evidence is needed to suggest modification and support a single-reference obviousness rejection. It is fundamental, as indicated in MPEP Section 2143.01, that the Examiner rely on some evidentiary quality suggestion to modify Rangan et al.:

> Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also >*In re Lee*, 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references);< *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The MPEP cites *In re Lee*, in which the Federal Circuit clarified the need for evidentiary quality support of an Examiner's factual basis for finding a teaching, suggestion or

motivation in the prior art (as opposed to the Examiner's opinion), 277 F.3d at 1343-44:

> As applied to the determination of patentability *vel non* when the issue is obviousness, "it is fundamental that rejections under 35 U.S.C. § 103 must be based on evidence comprehended by the language of that section." *In re Grasselli*, 713 F.2d 731, 739, 218 U.S.P.Q. (BNA) 769, 775 (Fed. Cir. 1983). ... "The factual inquiry whether to combine references must be thorough and searching." *Id.* It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with. [citation omitted] The need for specificity pervades this authority. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1371, 55 U.S.P.Q.2D (BNA) 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); *In re Rouffet*, 149 F.3d 1350, 1359, 47 U.S.P.Q.2D (BNA) 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); *In re Fritch*, 972 F.2d 1260, 1265, 23U.S.P.Q.2D (BNA) 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references"). ... In its decision on Lee's patent application, the Board rejected the need for "any specific hint or suggestion in a particular reference" to support the combination of the Nortrup and Thunderchopper references. Omission of a relevant factor required by precedent is both legal error and arbitrary agency action.

The outcome of cases decided even before *In re Lee* makes it clear that real evidence is required to support an asserted teaching, suggestion or motivation to modify a single reference for obviousness. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1369-70 (Fed. Cir. 2000) (rev'd finding of obviousness, as "Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference."); *Kolmes v. World Fibers Corp.*, 107 F.3d 1534, 1541 (Fed. Cir. 1997) (aff'd patent not invalid, as no suggestion to modify the '989 patent with regard to non-metallic fibers).

The Examiner's analysis thus far has not met the standard for a *prima facie* case of single reference obviousness.

Therefore, claim 1 should be allowable over Rangan et al.

Claim 2

Claim 2 includes the limitations:

an input for receiving an input signal;

an output configured to output a output signal;

a summation component configured to add a first error voltage value, which is derived from an output signal, to an incoming input signal; and

a subtraction component configured to subtract a second error voltage value, where the second error voltage value is derived from the adding of a first error voltage value to an incoming input signal.

These limitations are not found in Rangan et al.

Claim 2 is a device variation on method claim 1. It is even more explicit than claim 1 about identifying a "summation component configured to add" a first error value. This is the element that the Examiner acknowledges is missing from Rangan et al. For the reasons given above, modifying Rangan et al. using the claims of this application as a roadmap would involve an inventive effort. This claim is non obvious over Rangan et al. It would be very difficult and non obvious to redraw Rangan et al. FIG. 2 to read on this claim.

Therefore, claim 2 should be allowable over Rangan et al.

Claim 3

Claim 3 includes the limitations:

A sigma delta digital circuit according to Claim 2, further comprising a filter configured to filter an input signal according to a filter function, wherein the filter generates noise that distorts the filtered input signal, wherein the distortion results in the first error value.

These limitations are not found in Rangan et al.

The Examiner treats Rangan et al. ref. 12 as the first filter that generates noise that distorts the filter input signal. The application teaches a gain function that attenuates noise in the lower frequency ranges. That is not what Rangan et al. ref. 12 teaches. From Rangan et al., col. 3 lines16-29, "filter 12 forms a notch filter that substantially attenuates components of the digital signal 22 near one-half the sampling rate and passes substantially unattenuated components having frequencies outside of the notched filter."

Interposing the notch filter 12 in a negative feedback loop as taught by Rangan et al. does not read on claim 3.

Therefore, claim 3 should be allowable over Rangan et al.

Claim 4

Claim 4 includes the limitations:

> *A sigma delta digital circuit according to Claim 2, further comprising a filter configured to filter an input signal according to a filter function, wherein the filter generates noise that distorts the filtered input signal, wherein the distortion results in the second error value.*

These limitations are not found in Rangan et al.

In FIG. 1 of the application, the filter H(S) ref. 102 is positioned before quantization. It appears that the only reason that the Examiner is referring to adding an entirely new filter to Rangan et al., instead of selecting ref. 64 of the second order stage, is that feedback from ref. 64 if positive feedback instead of the claimed negative feedback.

It is nonsense to say that filters can always be added anywhere to improve the performance of any circuit (OA at 3-4). Even the purported teaching of Rangan et al. does not read on the claim limitations. The Examiner's conclusory statement is not enough to satisfy the *prima facie* burden, as articulated by *In re Lee* and the single-reference obviousness cases cited above.

Therefore, claim 4 should be allowable over Rangan et al.

Applicants respectfully submit that claims 1-4 should be allowable over Rangan et al.

CONCLUSION

Applicants respectfully submit that the pending claims are now in condition for allowance and thereby solicit acceptance of the claims as now stated.

Applicants would welcome an interview, if the Examiner is so inclined. The undersigned can ordinarily be reached at his office at (650) 712-0340 from 8:30 a.m. to 5:30 p.m. PST, Monday through Friday, and can be reached at his cell phone at (415) 902-6112 most other times.

Fee Authorization. The Commissioner is hereby authorized to charge any fee(s) determined to be due in connection with this communication to our Deposit Account No. 50-0869 (HBES 1071-2).

Respectfully submitted,

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